

Fig. 1

	11	10	9	8	7	6	5	4	3	2	1	0
Word 0	Rx_DV = 0	Rx_Cyc	Tx_Cyc	Mdout	00	PtM_mode	Even	CRS	Rx_Er			
Word 1					01	RST_RQST	SQL		Duplex	Speed	I_Er	
Word 2					10	rsrvd	rsrvd		rsrvd	Link	Int_rqst	

Fig. 2

11	10	9	8	7	6	5	4	3	2	1	0	
Rx_Dv = 1												
	Rx_Cyc = 1											
		Tx_Cyc										
			Rdata0	Rdata1	Rdata2	Rdata3	Rdata4	CRS	Rdata5	Rdata6	Rdata7	

Fig. 3

11	10	9	8	7	6	5	4	3	2	1	0
Rx_Dv = 1	Rx_Cyc = 1	Mdout	Rdata0	Rdata1	Rdata2	Rdata3	Rdata4	CRS	Rdata5	Rdata6	Rdata7

Fig. 4

11	10	9	8	7	6	5	4	3	2	1	0
Rx_Dv = 1	Rx_Cyc = 0	Tx_Cyc	Mdout	rsrvd	rsrvd	rsrvd	rsrvd	CRS	rsrvd	rsrvd	rsrvd

**Fig. 5**

11	10	9	8	7	6	5	4	3	2	1	0
SEL = 0	Mdstart	Mdin	Tx_EN = 1	Tdata0	Tdata1	Tdata2	Tdata3	Tdata4	Tdata5	Tdata6	Tdata7
			Tx_EN = 0	rsrvd	rsrvd	rsrvd	rsrvd	PHY_PD	Lpbk	LED_SEL	Rx_addr_match
SEL = 1	Command_Word										

**Fig. 6**

Mdin	IDLE	ST	OP	Reg Addr (10 bits)	Data (16 bits)
	000...0	1	01		
Mdout	IDLE				

Fig. 7

Mdin	IDLE	ST	OP	Reg Addr (10 bits)	Wait Time	IDLE
	000...0	1	10		0001	000...0
Mdout	IDLE				0001	Data (16 bits)

Fig. 8

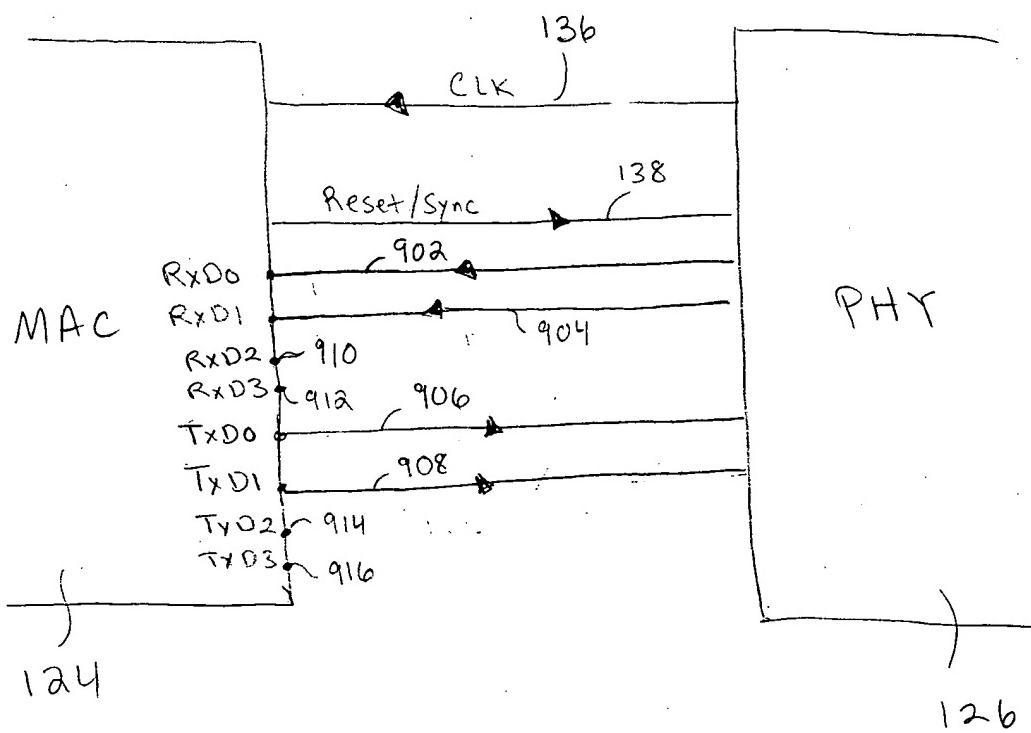


Fig. 9

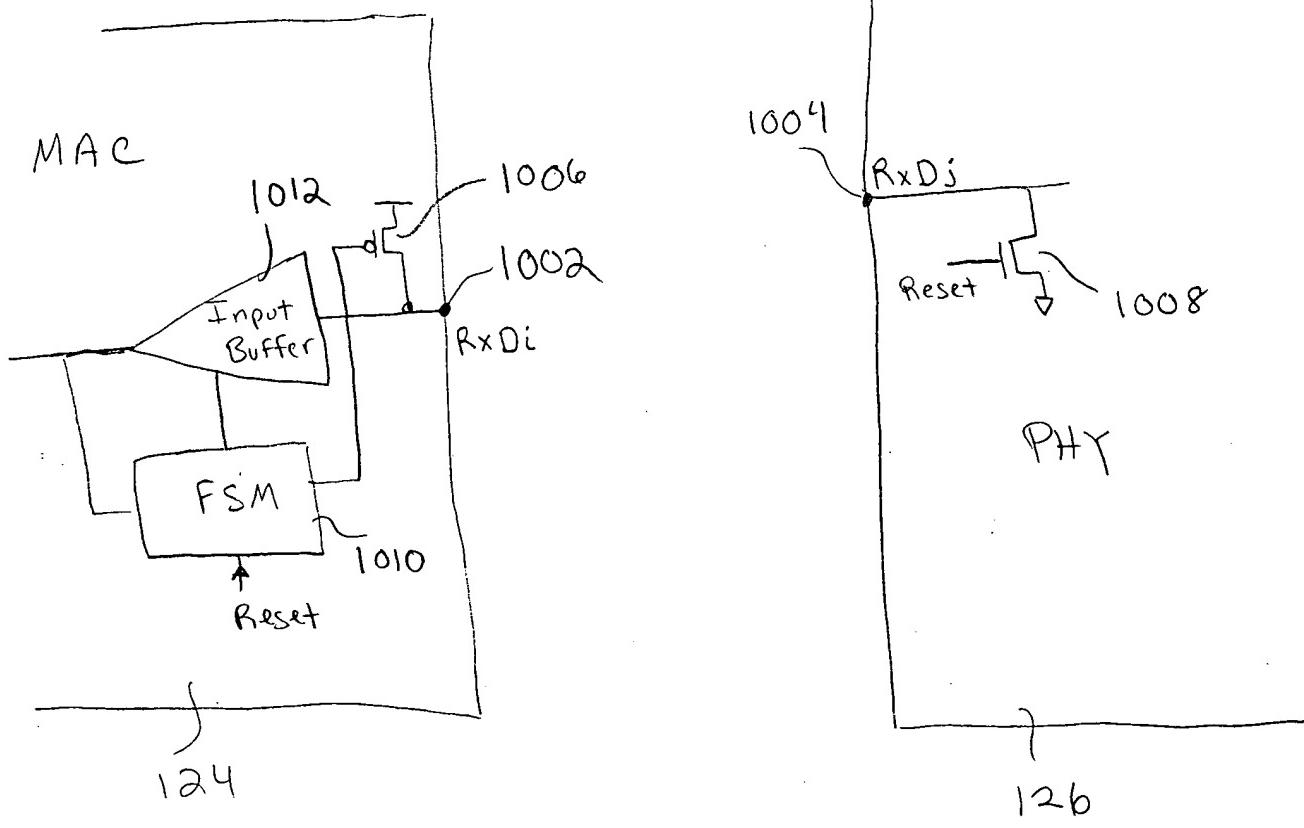


Fig. 10

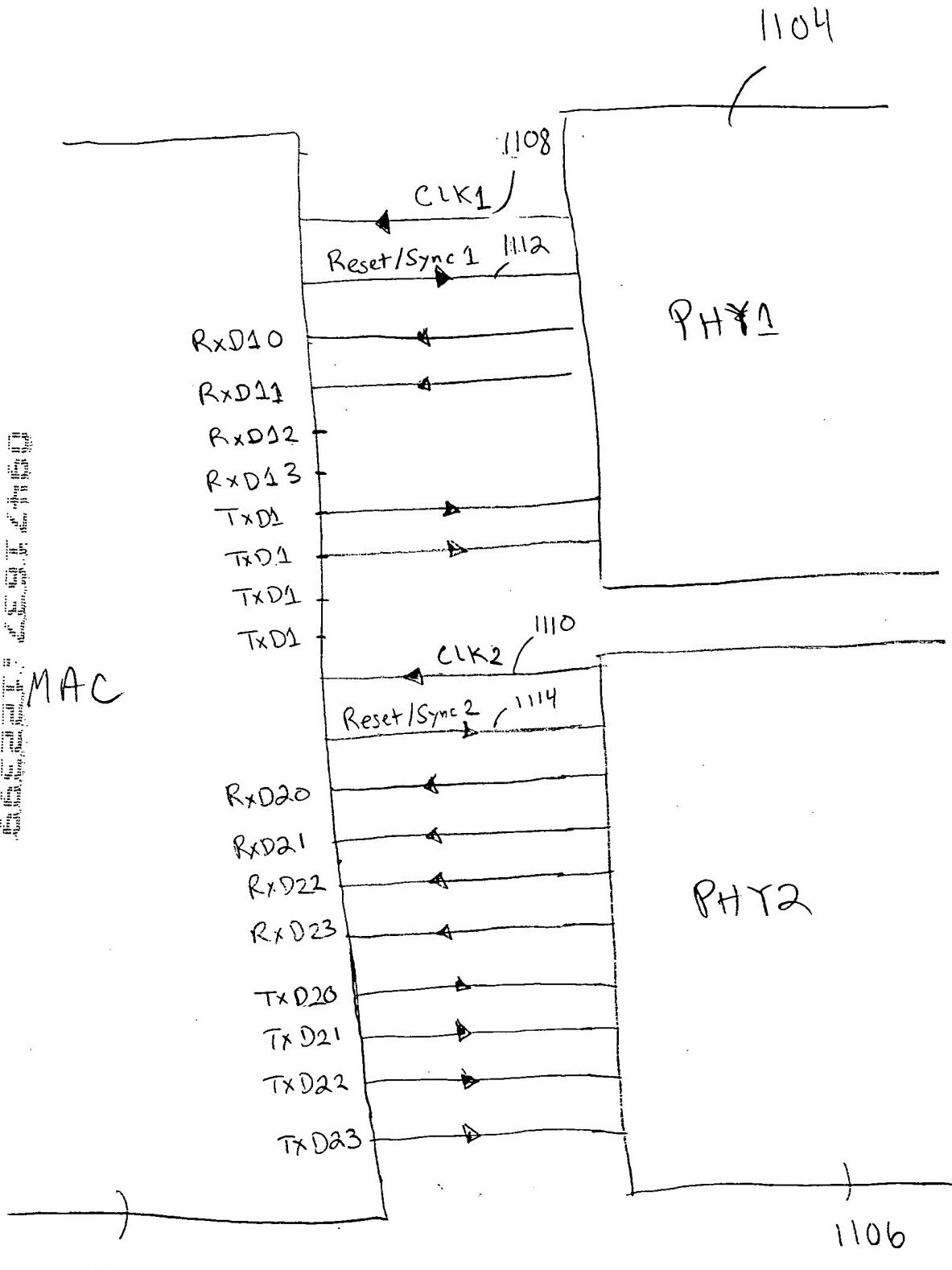


Fig. 11

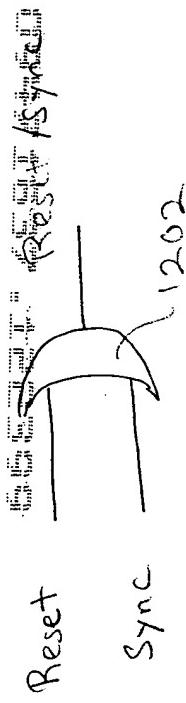


Fig. 12 a

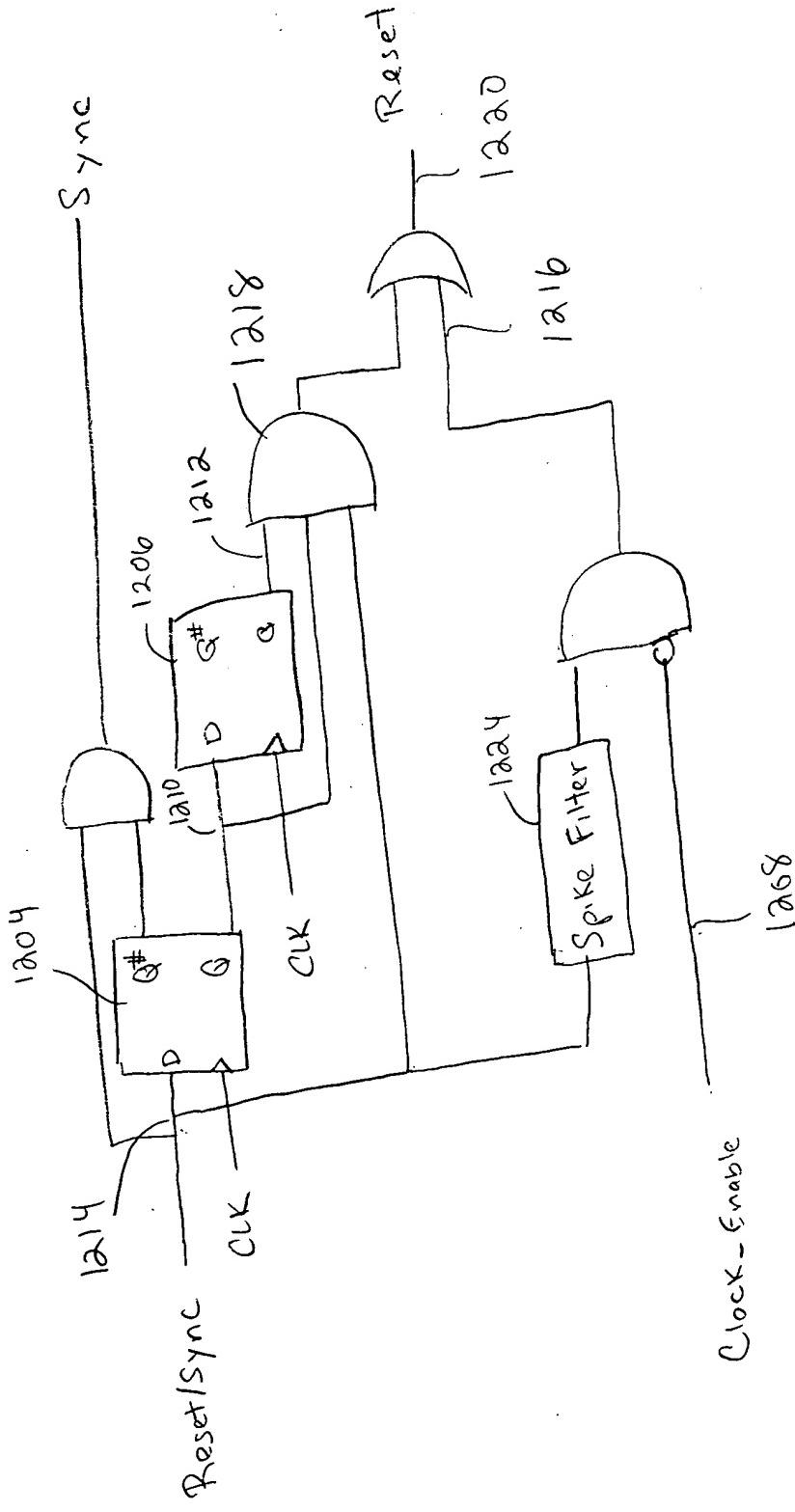


Fig. 12 b